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PERFORMANCE OF T FLIP FLOP USING CMOS 90 nm TECHNOLOGY

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T flip-flop.

Abstract

This paper presents designing T Flip Flop to redue power and area using 90nm Technology. Two designs for T Flip Flop have been proposed namely fully automatic and semi custom.In fully automatic design inbuilt active devices are used along with auto routing and placements. In semi custom design inbuilt active devices are used with optimized manual routing and placement. The proposed schematic in case of fully automatic approach is designed by using DSCH and its equivalent layout is created using microwind. While in the case of semi custom approach optimized layout is created with microwind. It can be observed from the simulated results that power is reduced by 76% and area consumption is improved by 9% in case of semi-custom design as compared to fully automatic design

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1. Introduction

Sequential circuits are circuits in which output is determined by current inputs as well as past inputs and thus they require memory. The combinational circuit don't use any memory. Hence the input of previous statedoesn't have any effect on the circuit's present state. Memory is present in sequential circuits so output can vary based on given input. Previous input, output, clock and a memory element are used by these type of circuits. Sequential circuit designs use flip-flops or latches, which are sometimes called memory elements that hold data. Sequential circuits are sorted as bistable, mono stable and astable.Bistable states have two stable states, either of them can be attained as per given conditions. Among the group of sequential circuits , the bistable circuits are the most popular ones. All basic elements like flip-flops, registers and memory elements fall in this category[1,2].

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Very-large-scale integration (VLSI) is the procedure of making an integrated circuit (IC) by integrating many transistors into a single chip. All basic elements like flip-flops, registers and memory elements fall in this category[3]. When VLSI technology wasn't introduced, ICs could only perform specific or limited set of functions. ICs have advantage of speed, size and power consumption over digital circuits. We have number of different IC fabrication technologies. The most important difference between technologies is the types of transistors they can produce[4]. MOSFETs offer the advantage of drawing almost zero control current while idle. They come in two variants: pMOS and nMOS using n- and p-type dopants respectively. An individual CMOS transistor consumes very little energy each time it switches on, the huge amount of transistors switching at very high speed rate makes power utilization a major design consideration. In this paper the estimation of SR flip-flop's performance is done based on area measured.

T Flip Flop or Toggle Flip – flop is made to prevent the upcoming intermediate state in SR flip – flop, only one input is provided to the flip – flop called Trigger input or Toggle input (T). This flip – flop performs similar to as a Toggle switch. Toggling means to toggle or to change the next state output to complement the present state output.

Design of T flip – flop can be made by simply making modifications to JK flip – flop. The T flip – flop is a single input device, thus by connection of J and K inputs together and providing them single input called T, a JK flip – flop is converted into T flip – flop. So a T flip – flop is also called single input JK flip – flop.

The logical diagram of T flip – flop is shown below. It has one Toggle input (T) & one clock signal input (CLK).

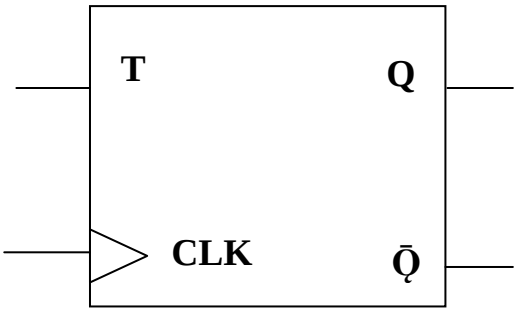

Figure 1. Symbol of T Flip Flop

The Truth table of T flip flop is also shown as Table 1

T	Q_n	Q_{n+1}
0	0	0
1	0	1
0	1	1
1	1	0

Table 1.Truth Table of T Flip-Flop

The characterstic equation of T Flip Flop is given by:

$$Q_{n+1}=T\,\bar{Q}_n + T'$$

2. Objective of Study:

To reduce the power consumed and area covered by the circuit to give the desired result.

3. Research Method:

The easiest of the schematic of a T flip – flop is with JK flip – flop. The J and K input of the JK flip – flop are connected with each otherr and given the T input. The logic circuit hence created of T flip – flop from a JK flip – flop is shown below in Figure 2 as a schematic in DSCH.

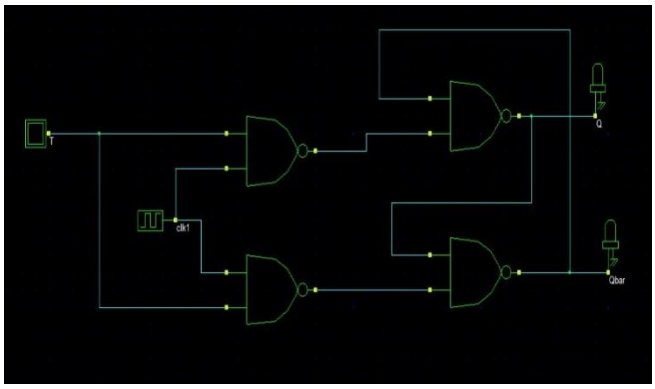

Figure 2. Diagram of NAND-based T flip flop circ

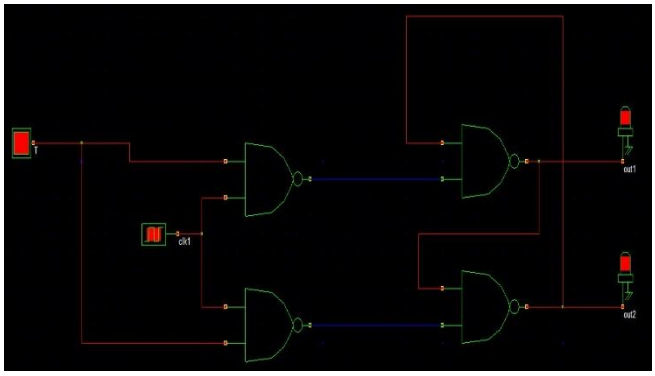

Figure 3.Simulation of Nand based T Flip Flop

JK flip flop's modified form results in T Flip Flop. The Q and $\bar{Q}$ represents the output states of the flip-flop. Accordingly, based on the input the output changes its state. All these can occur only in the presence of the clock signal. Thus, works unlike to SR flip Flop & JK flip-flop for the complimentary inputs. T Flip Flop only has this toggling feature.

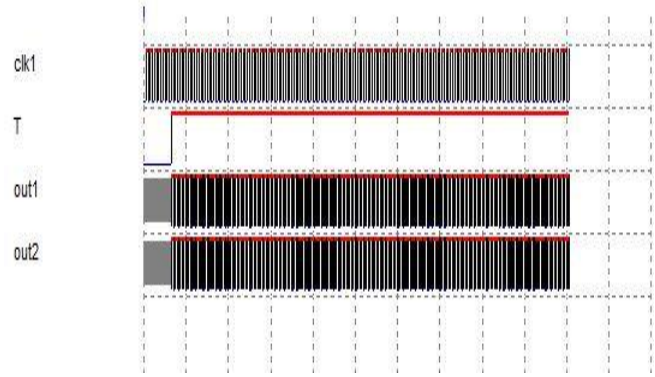

Figure 4. Timing diagram of fully automatic

In first method the schematic of SR flip-flop is designed, with the help of Microwind software the auto generated layout of SR flip-flop is created, afterwards simulation is done. In this, 90nm foundary is selected. The figure 2 represents the auto generated layout

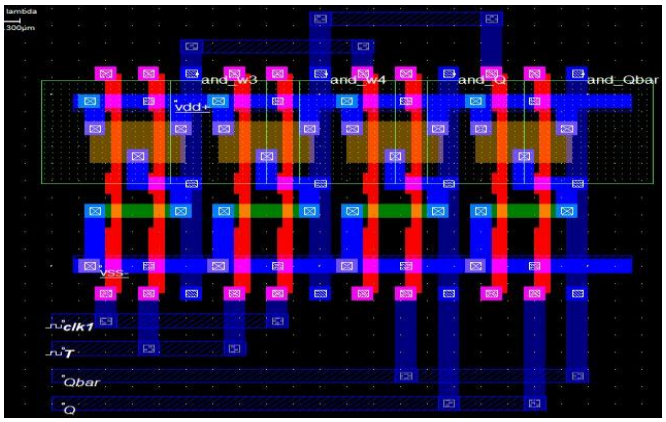

Figure 2. Auto generated SR flip-flop

The layout is checked for DRC and if there no error is generated then simulated result appears. Later generated timing waveforms are verified by comparing to the circuit operation. The power generated is shown by the simulated result. The figure 3 shows the timing diagram of this automatic layout.

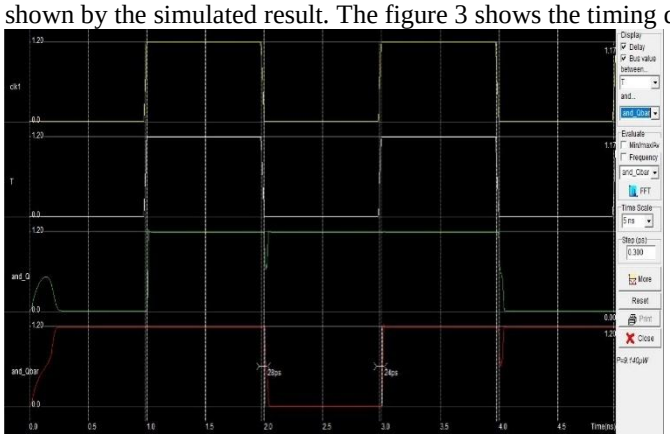

Figure 3. Timing Diagram of Automatic Generated Layout

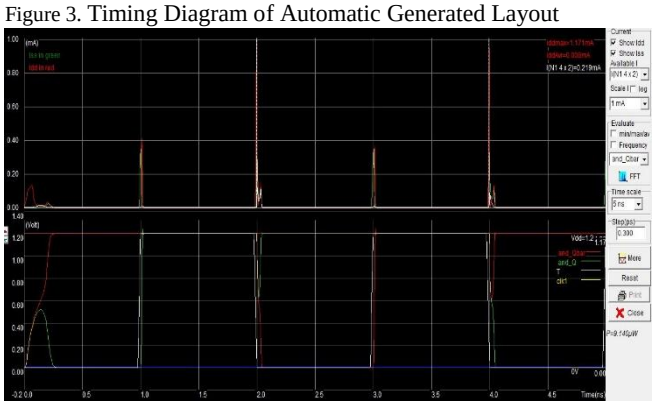

Figure 4. Voltage vs Current graph for fully automatic

The power and area consumed by this layout is measured. Here the consuming power is 9.140 µW. Area required for this particular layout is 47.6 μm^2. Width is 6.8µm (114 lambda) and height is 7.0µm (116 lambda).

Secondly we prepare layout using semicustom approach. In semicustom approach the transistors are inbuilt, In this approach connections are made by following the lambda design rules. There is slight possibility of power reduction. Figure 5 represents the layout using semicustom approach

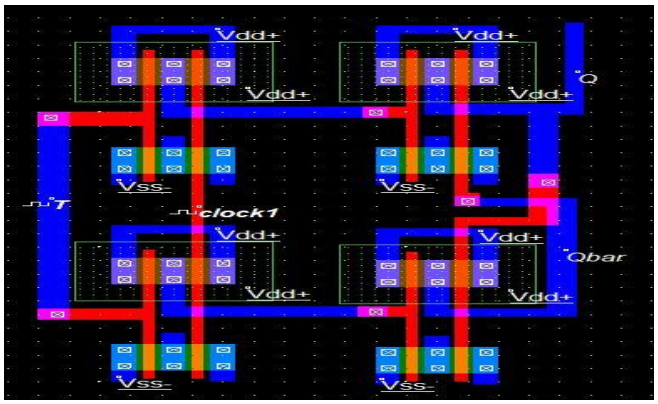

Figure 5 Semi custom Layout of T flip-flop

Checking of DRC is done in semi custom layout and if there is no error present in the layout, the circuit is simulated successfully and respective results are generated as timing waveforms. Verification of generated timing waveforms are done with the truth table or operation of original circuit. Figure 6 shows the timing diagram of semicustom layout.

Further voltage and current relation in semi custom layout is simulated to get the comparison of current and voltage. Figure 7 shows the simulated relationship.

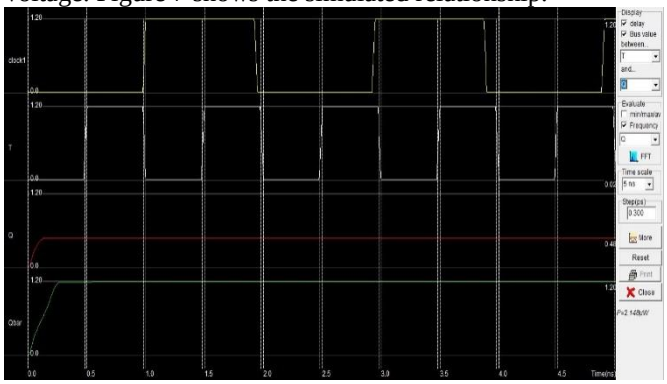

Figure 6. Timing diagram of semi custom layout

The power observed from this particular simulation done in Figure 6, is 2.148 µWatt, more than automatic layout. And area is calculated from the properties. Here the width is 5.3 µm (89 lambda) and height is 8.0 µm (134 lambda). In semicustom layout area is 42.9 μm^2

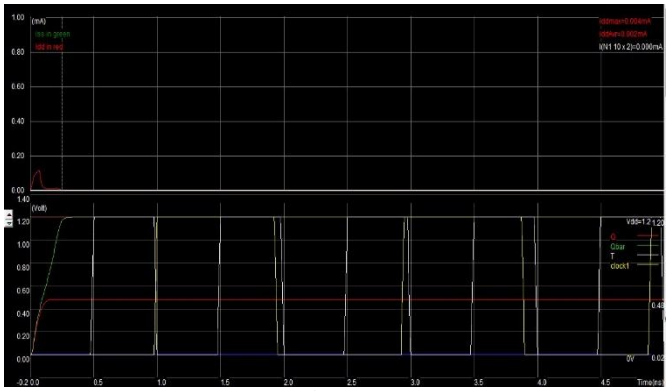

Figure 7. Voltage vs Current graph for semi custom design

4. Results and Analysis

The performance of proposed semi custom layout is compared with automated layout. The performance parameters being Area and Power. Through above results a
comparative study can be done between the two designing approaches. Table 2 shows the comparative analysis.

Approach	Area(μm^2)	Power(µWatt)
Fully Automatic	47.6 μm^2	9.140 µWatt
Semi custom	42.9 μm^2	2.148 µWatt

Table 2 Analysed Table

Comparative analysis table shows power of semi automatic layout approach decreases. In terms of area the semi custom layout has better performance among the two design approaches.

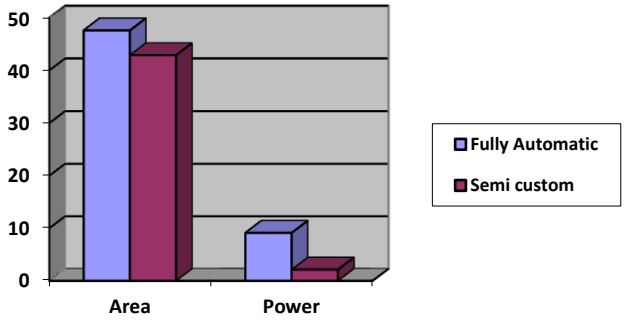

Figure. 8Bar graph Comparison

From the above comparison we observed, there is a reduction of 76% in power for semicustom layout generated in comparison to fully automatic layout and reduction of 9% in terms of area consumed. More area is required in auto generated approach. Comparative analysis in terms of area is done, which indicates that semi customized layouts have less area than auto generated.

5. Conclusion

Through above result analysis it is clear that semi customized layout is better than auto generated layout by 6.992 µW in terms of power and 4.7μm^2 better in terms of area consumption.

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